UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/870,280	05/30/2001	Mojdeh Shakeri	04899-050001	7303

959 7590 07/19/2005

LAHIVE & COCKFIELD, LLP.
28 STATE STREET
BOSTON, MA 02109

EXAMINER	
STEVENS, THOMAS H	

ART UNIT	PAPER NUMBER
2123	

DATE MAILED: 07/19/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/870,280	SHAKERI ET AL.	
	Examiner	Art Unit	
	Thomas H. Stevens	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 June 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-36* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *5/30/01* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Section I: Response to Applicants' Arguments (Final Office Action)

35 U.S.C. 103

1. Applicants are thanked for addressing this issue. Rejection is withdrawn.

Section II: Non-Final Rejection (RCE—First Office Action)

Drawings

2. New corrected drawings in compliance with 37 CFR 1.121(d) is required in this application because some of the notations are unclear to read. Applicant is advised to employ the services of a competent patent draftsperson outside the Office, as the U.S. Patent and Trademark Office no longer prepares new drawings. The corrected drawings are required in reply to the Office action to avoid abandonment of the application. The requirement for corrected drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-26, 28-36 are rejected under 35 U.S.C. 102(b) as being anticipated by Deb et al., (Multi-Signal Graphs: A Novel Approach for System Testability Analysis and Fault Diagnosis (1995)). Deb et al. discloses modeling multi-signal directed graphs that correspond closely to hierarchical system schematics (abstract).

Claim 1. A modeling process comprising: providing a plurality of blocks (Deb: pg. 6,figure 4 (elements s1-s5) and section 2.5.2), each of the block (Deb: pg. 6,figure 4 (elements s1-s5) and section 2.5.2)) representing functional entities (Deb: pg. 6, figure 4 with section 2.5.5); generating a plurality of output signal values from the plurality of blocks (Deb: pg. 6,figure 4 (elements s1-s5) and section 2.5.2) and section 2.5.2); grouping the plurality of output signal values as an ordered set in a multiplexer as a first composite signal (Deb: pg. 6,figure 4 (elements s1-s5) and section 2.5.2); and outputting the first composite signal (Deb: pg. 6,figure 4 (elements s1-s5) and section 2.5.2).

Claim 2. The process of claim 1 (Deb: pg. 6,figure 4 (elements s1-s5)) wherein each of the blocks (Deb: pg. 6,figure 4 (elements s1-s5) and section 2.5.2) includes at least one output signal port.

Claim 3. The process of claim 1(Deb: pg. 6,figure 4 (elements s1-s5)) wherein a plurality of input signal values and the output signal values have at least one attribute (pg. 6, figure: e.g., "Midrange, Power Amp).

Claim 4. The process of claim 3 (Deb: pg. 6,figure 4 (elements s1-s5; pg. 6, figure: e.g., "Midrange, Power Amp)) wherein the attribute is a name (pg. 6, figure: e.g., "Midrange, Power Amp).

Claim 5. The process of claim 3, (Deb: pg. 6,figure 4 (elements s1-s5; pg. 6, figure: e.g., "Midrange, Power Amp)) wherein the attribute is a data type.

Claim 6. The process of claim 3 (Deb: pg. 6,figure 4 (elements s1-s5; pg. 6, figure: e.g., "Midrange, Power Amp)) wherein the attribute is numeric type.

Claim 7. The process of claim 3, (Deb: pg. 6,figure 4 (elements s1-s5; pg. 6, figure: e.g., "Midrange, Power Amp)) wherein the attribute is a dimensionality.

Claim 8. The process of claim 1(Deb: pg. 6,figure 4 (elements s1-s5)) wherein the ordered set is a linked list data structure (pg. 6, section 2.5.2 with figure 4 and tables 2 and 3).

Claim 9. The process of claim 8 (Deb: pg. 6,figure 4 (elements s1-s5) wherein the linked list data structure is a tree (pg. 2, left column with figure 1 and right column, 1st paragraph) data structure, the tree (pg. 2, left column with figure 1 and right column, 1st paragraph) data structure including m + n nodes (Deb: pg. 3, right column, 3rd paragraph; pg. 8, left column, paragraphs 1-5).

Claim 10. The process of claim 9, (Deb: pg. 6,figure 4 (elements s1-s5) wherein m represents a number of independent signals and n represents a number of composite signals (Deb: pg. 6,figure 4 (elements s1-s5) and section 2.5.2).

Claim 11. The process of claim 1 (Deb: pg. 6,figure 4 (elements s1-s5)) further comprising decomposing the first composite signal (Deb: pg. 6,figure 4 (elements s1-s5) and section 2.5.2) into the plurality of output signals in a demultiplexer.

Claim 12. The process of claim 1(Deb: pg. 6,figure 4 (elements s1-s5)) further comprising viewing the ordered set contained in the first composite signal (Deb: pg. 6,figure 4 (elements s1-s5) and section 2.5.2) with a composite signal (Deb: pg. 6,figure 4 (elements s1-s5) and section 2.5.2) viewer.

Claim 13. The process of claim 1 (Deb: pg. 6,figure 4 (elements s1-s5)) herein at least one of the input signal values is a second composite signal (Deb: pg. 6,figure 4 (elements s1-s5) and section 2.5.2).

Claim 14. A block (Deb: pg. 6,figure 4 (elements s1-s5) and section 2.5.2) diagram modeling process comprising: providing a first block (Deb: pg. 6,figure 4 (elements s1-s5) and section 2.5.2) and a second block (Deb: pg. 6,figure 4 (elements s1-s5) and section 2.5.2), the blocks (Deb: pg. 6,figure 4 (elements s1-s5) and section 2.5.2) (Deb: pg. 6,figure 4 (elements s1-s5) and section 2.5.2) representing functional entities; generating a plurality of output signal values from the first and second block (Deb: pg. 6,figure 4 (elements s1-s5) and section 2.5.2); grouping the plurality of output signal values as an ordered set in a multiplexer as a first composite signal (Deb: pg. 6,figure 4 (elements s1-s5) and section 2.5.2) ; and

processing the composite signal (Deb: pg. 6,figure 4 (elements s1-s5) and section 2.5.2) in a third block (Deb: pg. 6,figure 4 (elements s1-s5) and section 2.5.2)

Claim 15. The process of claim 14 (Deb: pg. 6,figure 4 (elements s1-s5) and section 2.5.2) wherein the ordered set is a linked list data structure (pg. 6, section 2.5.2 with table 3).

Claim 16. The process of claim 14 (Deb: pg. 6,figure 4 (elements s1-s5) and section 2.5.2) wherein an input signal is a second composite signal (Deb: pg. 6,figure 4 (elements s1-s5) and section 2.5.2).

Claim 17. The process of claim 14 (Deb: pg. 6,figure 4 (elements s1-s5) and section 2.5.2) further comprising decomposing the composite signal (Deb: pg. 6,figure 4 (elements s1-s5) and section 2.5.2) into a plurality of input signal values (Deb: pg. 6,figure 4 (elements s1-s5) and section 2.5.2: output of "Light")

Claim 18. The process of claim 14, (Deb: pg. 6,figure 4 (elements s1-s5) and section 2.5.2) wherein at least one of the input signals is a second composite signal (Deb: pg. 6,figure 4 (elements s1-s5) and section 2.5.2).

Claim 19. The process of claim 18 (Deb: pg. 6,figure 4 (elements s1-s5) and section 2.5.2) wherein the composite signal (Deb: pg. 6,figure 4 (elements s1-s5)

and section 2.5.2) viewer displays the ordered set contained in the composite signal (Deb: pg. 6,figure 4 (elements s1-s5) and section 2.5.2) on a graphical user interface (GUI).

Claim 20. The process of claim 19, (Deb: pg. 6,figure 4 (elements s1-s5) and section 2.5.2) wherein the GUI is provided on an input/output device.

Claim 21. A computer program product (inherent properites platform: Deb: pg. 1, right column, 2nd bullet) residing on a computer readable medium having instructions stored thereon which, when executed by the processor, cause the processor to: provide a plurality of blocks (Deb: pg. 6,figure 4 (elements s1-s5) and section 2.5.2), each of the block (Deb: pg. 6,figure 4 (elements s1-s5) and section 2.5.2) representing functional entities; generate a plurality of output signal values from the plurality of block (Deb: pg. 6,figure 4 (elements s1-s5) and section 2.5.2)s (Deb: pg. 6,figure 4 (elements s1-s5) and section 2.5.2)); group the plurality of output signal values as an ordered set in a multiplexer as a first composite signal (Deb: pg. 6,figure 4 (elements s1-s5) and section 2.5.2); and output the first composite signal (Deb: pg. 6,figure 4 (elements s1-s5) and section 2.5.2).

Claim 22. The computer program product (inherent properties platform: Deb: pg. 1, right column, 2nd bullet) of claim 21 (Deb: pg. 6,figure 4 (elements s1-s5) and

section 2.5.2) wherein the computer readable medium is a random access memory (RAM) (Inherent: common among modern computer hardware).

Claim 23. The computer program of claim 21 (inherent properties platform: Deb: pg. 1, right column, 2nd bullet) wherein the computer readable medium is read only memory (ROM) (Inherent: common among modern computer hardware).

Claim 24. The computer program of claim 21 (inherent properties platform: Deb: pg. 1, right column, 2nd bullet) wherein the computer readable medium is hard disk drive (Inherent: common among modern computer hardware).

Claim 25. A processor and a memory configured to: provide a plurality of blocks (Deb: pg. 6,figure 4 (elements s1-s5) and section 2.5.2), each of the blocks (Deb: pg. 6,figure 4 (elements s1-s5) and section 2.5.2) representing functional entities; generate a plurality of output signal values from the plurality of blocks (Deb: pg. 6,figure 4 (elements s1-s5) and section 2.5.2) and section 2.5.2); group the plurality of output signal values as an ordered set in a multiplexer as a first composite signal (Deb: pg. 6,figure 4 (elements s1-s5) and section 2.5.2); and output the first composite signal (Deb: pg. 6,figure 4 (elements s1-s5) and section 2.5.2).

Claim 26. The processor and memory of claim 25 (Deb: pg. 6,figure 4 (elements s1-s5) and section 2.5.2) wherein the processor and the memory are incorporated into a personal computer (Inherent to modern computer hardware).

Claim 28. The processor and memory of claim 25 (Deb: pg. 6,figure 4 (elements s1-s5) and section 2.5.2) wherein the processor and the memory are incorporated into a single board computer (Inherent to modern computer hardware).

Claim 29. A modeling process comprising: providing a plurality of blocks (Deb: pg. 6,figure 4 (elements s1-s5) and section 2.5.2), each of the blocks (Deb: pg. 6,figure 4 (elements s1-s5) and section 2.5.2) representing a functional entity that generates one or more output signals; grouping the output signals as an ordered set in a multiplexer as a composite signal (Deb: pg. 6,figure 4 (elements s1-s5) and section 2.5.2); and outputting the composite signal (Deb: pg. 6,figure 4 (elements s1-s5) and section 2.5.2).

Claim 30. The process of claim 29 (Deb: pg. 6,figure 4 (elements s1-s5) and section 2.5.2) wherein the ordered set is a tree (pg. 2, left column with figure 1 and right column, 1st paragraph) data structure.

Claim 31. The process of claim 30 (Deb: pg. 6,figure 4 (elements s1-s5) and section 2.5.2) wherein the tree (pg. 2, left column with figure 1 and right column, 1st

paragraph) data structure is a linked list (pg. 6, section 2.5.2 with figure 4 and tables 2 and 3).

Claim 32. The process of claim 29 (Deb: pg. 6,figure 4 (elements s1-s5) and section 2.5.2) further comprising: providing a composite signal (Deb: pg. 6,figure 4 (elements s1-s5) and section 2.5.2) viewer; and viewing the ordered set in a graphical user interface executing in the composite signal (Deb: pg. 6, figure 4 (elements s1-s5) and section 2.5.2) viewer.

Claim 33. A computer program product (inherent properties platform: Deb: pg. 1, right column, 2nd bullet) residing on a computer readable medium having instructions stored thereon which, when executed by the processor, cause the processor to: provide a plurality of blocks (Deb: pg. 6,figure 4 (elements s1-s5) and section 2.5.2) (Deb: pg. 6,figure 4 (elements s1-s5) and section 2.5.2), each of the blocks (Deb: pg. 6,figure 4 (elements s1-s5) and section 2.5.2) representing a functional entity that generates one or more output signal values; group the output signals as an ordered set in a multiplexer as a composite signal (Deb: pg. 6,figure 4 (elements s1-s5) and section 2.5.2); and output the composite signal (Deb: pg. 6,figure 4 (elements s1-s5) and section 2.5.2).

Claim 34. A processor and memory configured to provide a plurality of blocks (Deb: pg. 6,figure 4 (elements s1-s5) and section 2.5.2), each of the block (Deb: pg.

6,figure 4 (elements s1-s5) and section 2.5.2) a functional entity that generates one or more output signal values; group the output signals as an ordered set in a multiplexer as a composite signal (Deb: pg. 6,figure 4 (elements s1-s5) and section 2.5.2); and output the composite signal (Deb: pg. 6,figure 4 (elements s1-s5) and section 2.5.2).

Claim 35. A method for providing a composite signal (Deb: pg. 6,figure 4 (elements s1-s5) and section 2.5.2) in a modeling signal in a modeling environment, the method comprising the steps of: providing a plurality of output signals form one or more block (Deb: pg. 6,figure 4 (elements s1-s5) and section 2.5.2): generating a composite signal (Deb: pg. 6,figure 4 (elements s1-s5) and section 2.5.2) comprising a set of the plurality of output signals; and providing the composite signal (Deb: pg. 6,figure 4 (elements s1-s5) and section 2.5.2) as an output signal.

Claim 36. A method for graphically representing a composite signal (Deb: pg. 6,figure 4 (elements s1-s5) and section 2.5.2) in a modeling environment, the method comprising the steps of: providing a plurality of output signals from one or more blocks (Deb: pg. 6,figure 4 (elements s1-s5) and section 2.5.2), each output signal graphically indicated by a signal identifier; and providing a composite signal (Deb: pg. 6,figure 4 (elements s1-s5) and section 2.5.2) identifier representing a composite signal (Deb: pg. 6,figure 4 (elements s1-s5) and section 2.5.2) comprising a set of the plurality of output signals.

Claim Rejections - 35 USC § 103

5. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claim 27 is rejected under 35 U.S.C. 103 (a) as obvious by Deb et al., (Multi-Signal Graphs: A Novel Approach for System Testability Analysis and Fault Diagnosis (1995)), in view of Ghoshal et al., (Multi-signal Modeling for Diagnosis, FMECA, and

Reliability (1998)). Deb et al. discloses modeling multi-signal directed graphs that correspond closely to hierarchical system schematics (abstract);but doesn't teach applying this mode to the Internet. Ghoshal et al., teaches multi-signal modeling methodology (abstract) with Internet capabilities (pg.3031, left column, 2nd paragraph with figure 3).

At the time of invention, it would have been obvious to one of ordinary skill in the art to modify Deb et al, by way of Ghoshal et al., to promote universal sharing of model information (Ghoshal: pg. 3021, left column, 2nd paragraph, lines 8-10).

Claim 27. The processor and memory of claim 25 (Deb: pg. 6,figure 4 (elements s1-s5) and section 2.5.2) wherein the processor and the memory are incorporated into a network server residing in the Internet (Ghoshal: pg.3031, left column, 2nd paragraph with figure 3).

Correspondence Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mr. Tom Stevens whose telephone number is 571-272-3715, Monday-Friday (8:00 am- 4:30 pm) or contact Supervisor Mr. Leo Picard at (571) 272-3749. Central Fax number is 571-273-8300.

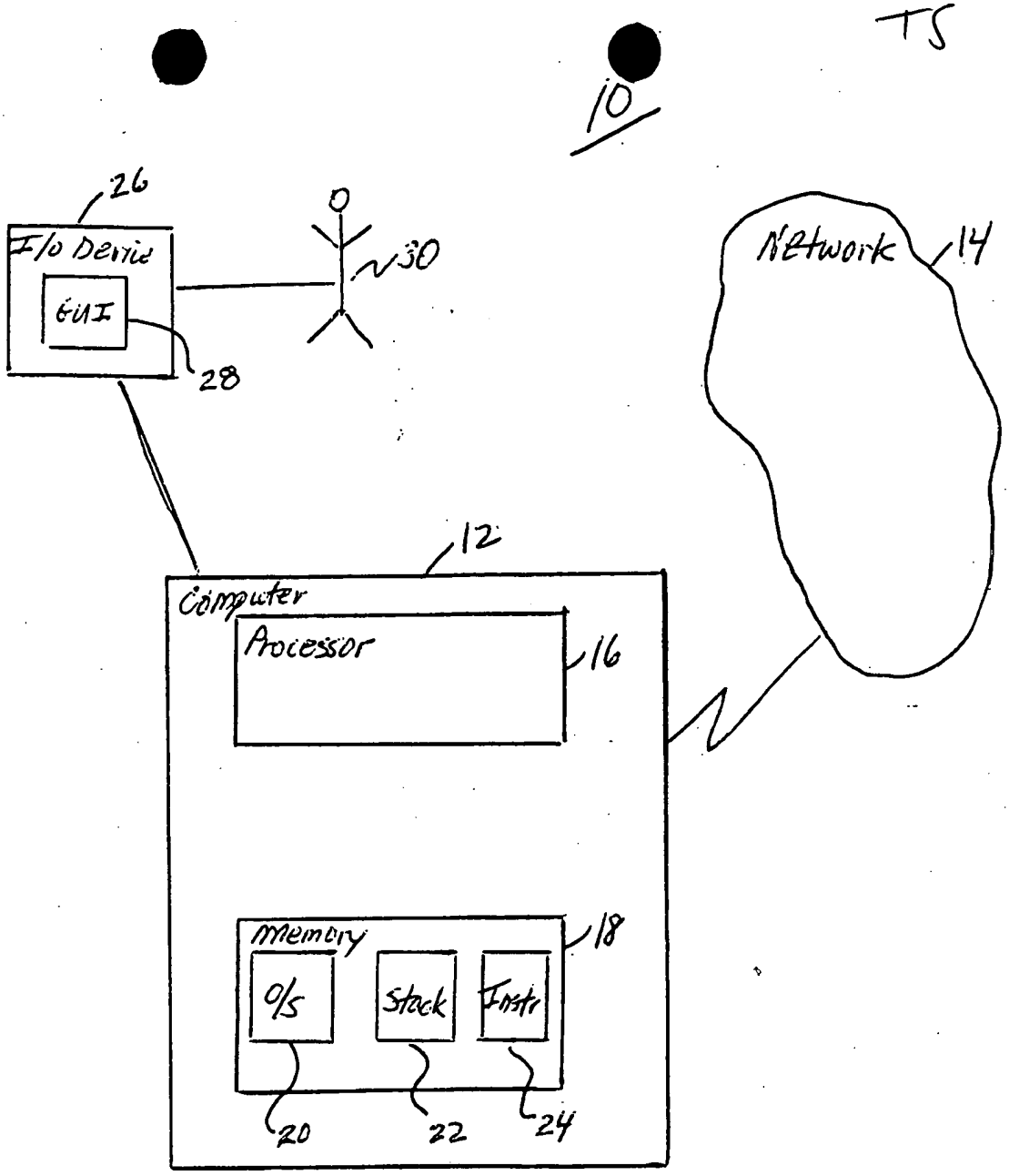
Any inquiry of a general nature or relating to the status of this application should be directed to the TC 2100 Group receptionist: 571-272-2100.

July 11, 2005

THS

LEO PICARD
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

TS



Block sim or sym

FIG. 1

50

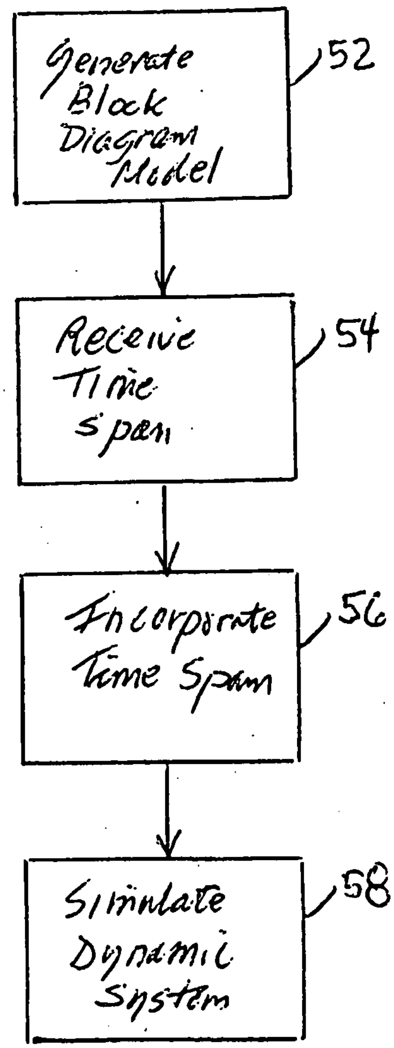


FIG. 2

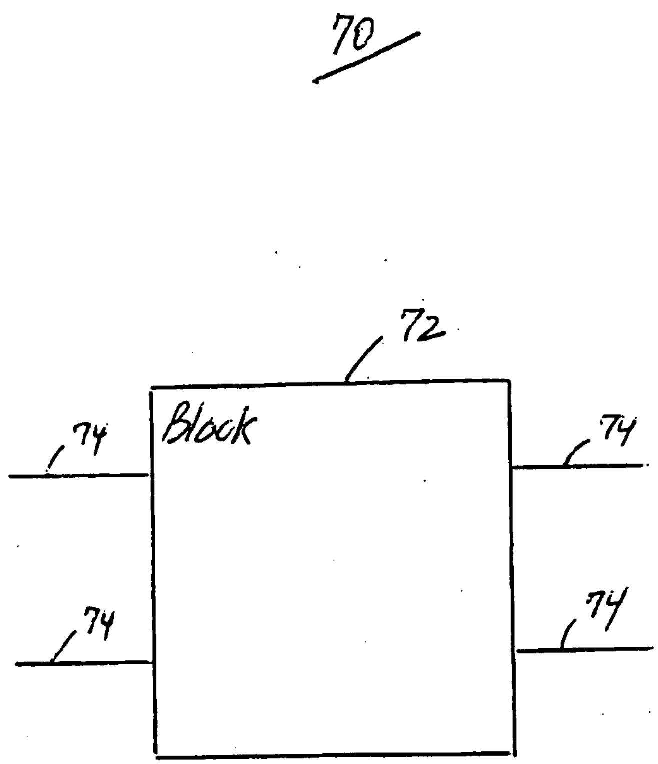


FIG. 3

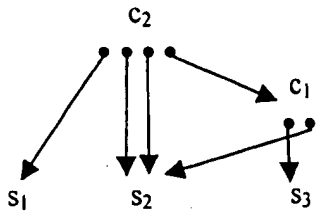


FIG. 4

77

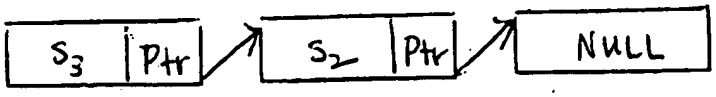


FIG. 5A

78

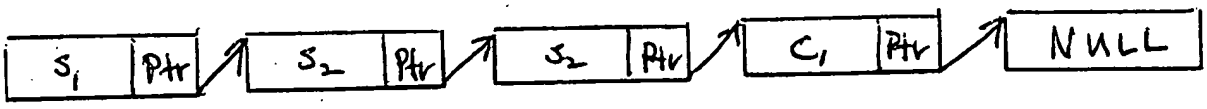


FIG. 5B

80

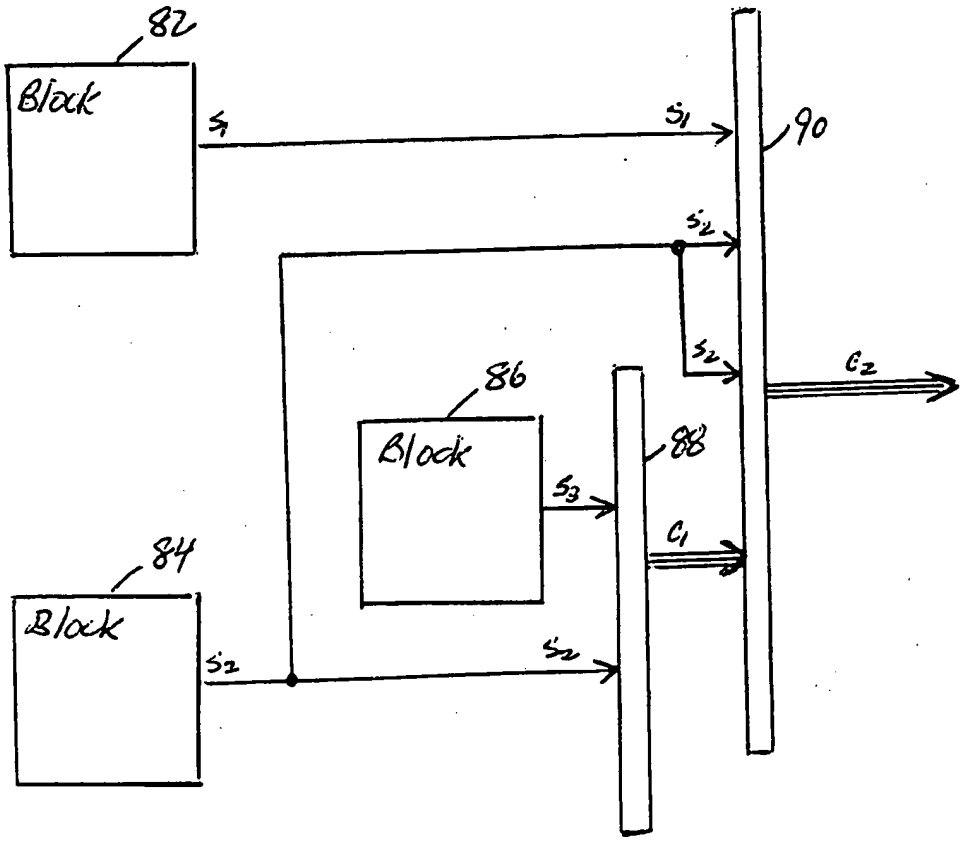


FIG. 6

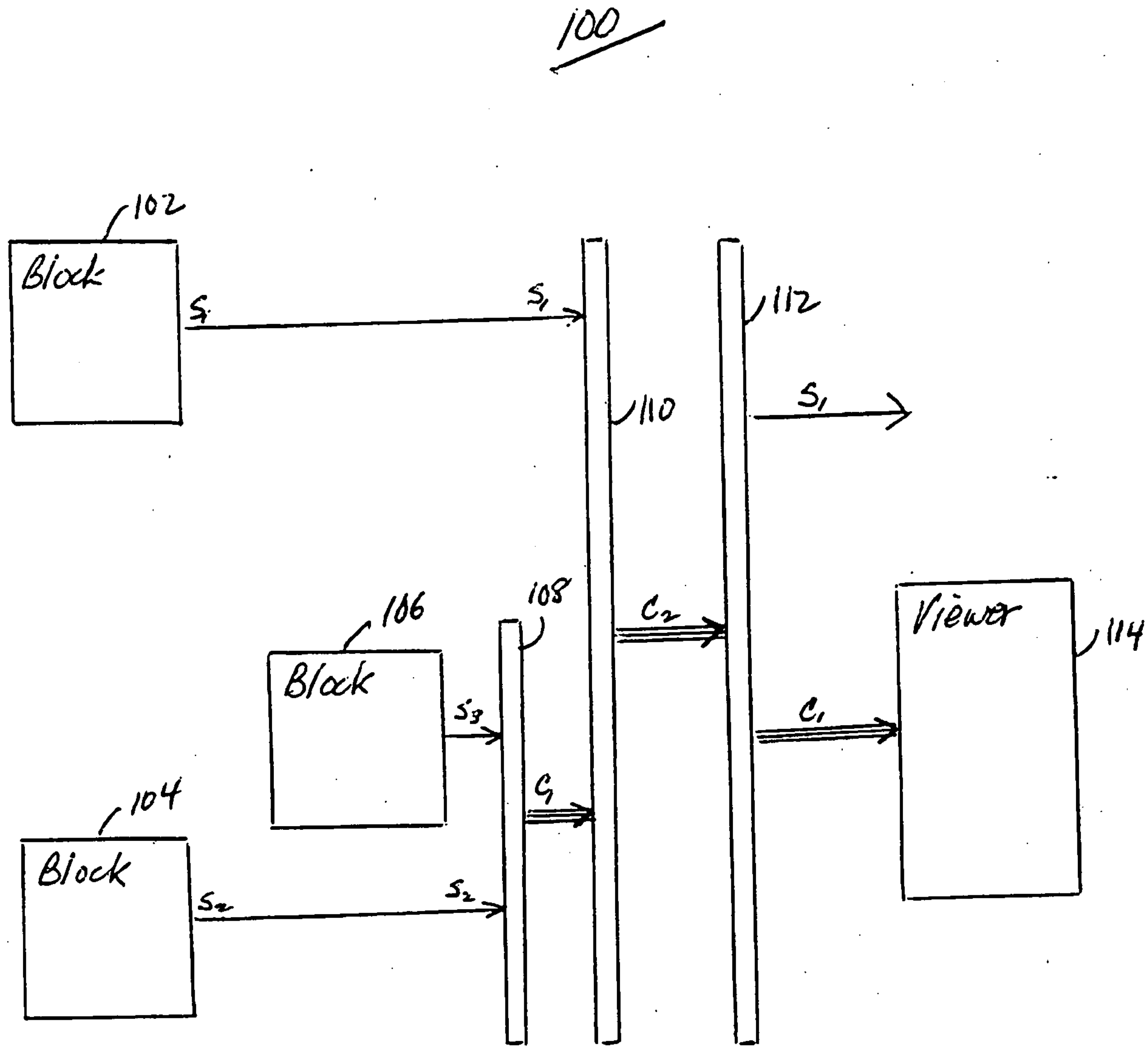


FIG. 7

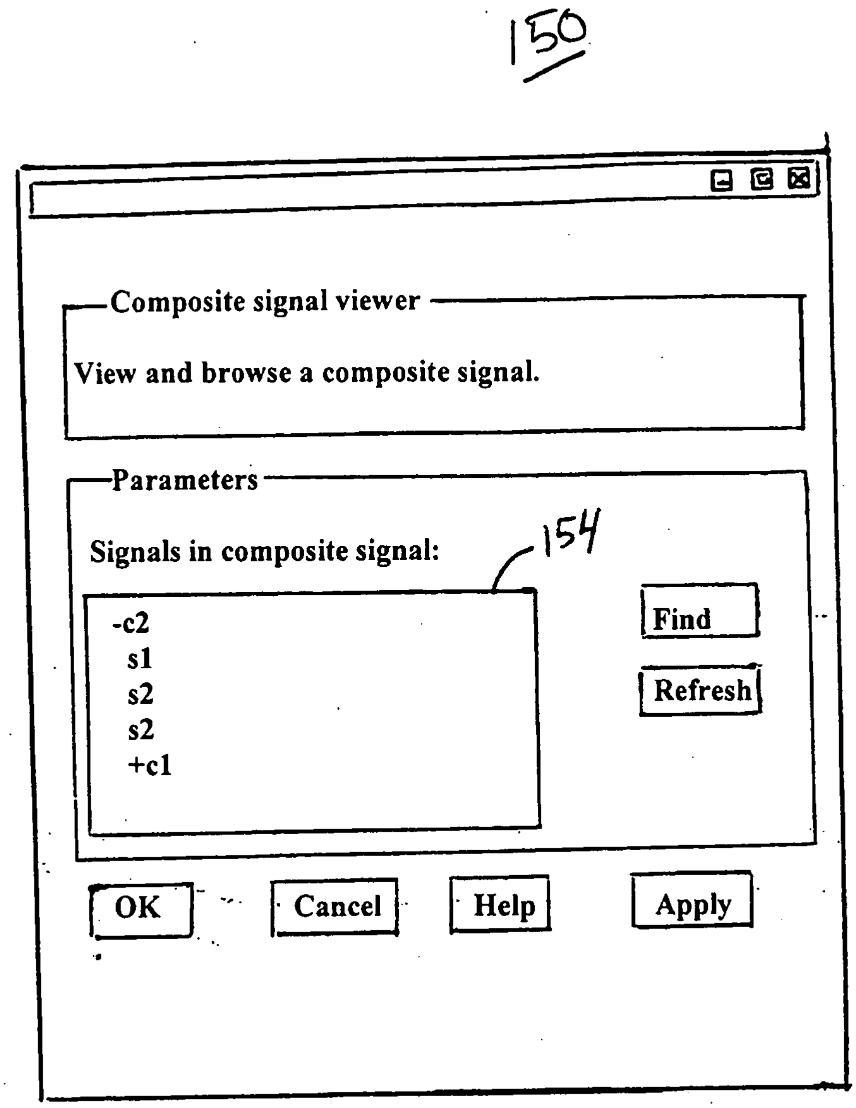

150
Composite signal viewer
View and browse a composite signal.
Parameters
Signals in composite signal:
154
-c2
s1
s2
s2
+c1
Find
Refresh
OK
Cancel
Help
Apply

FIG. 8

150

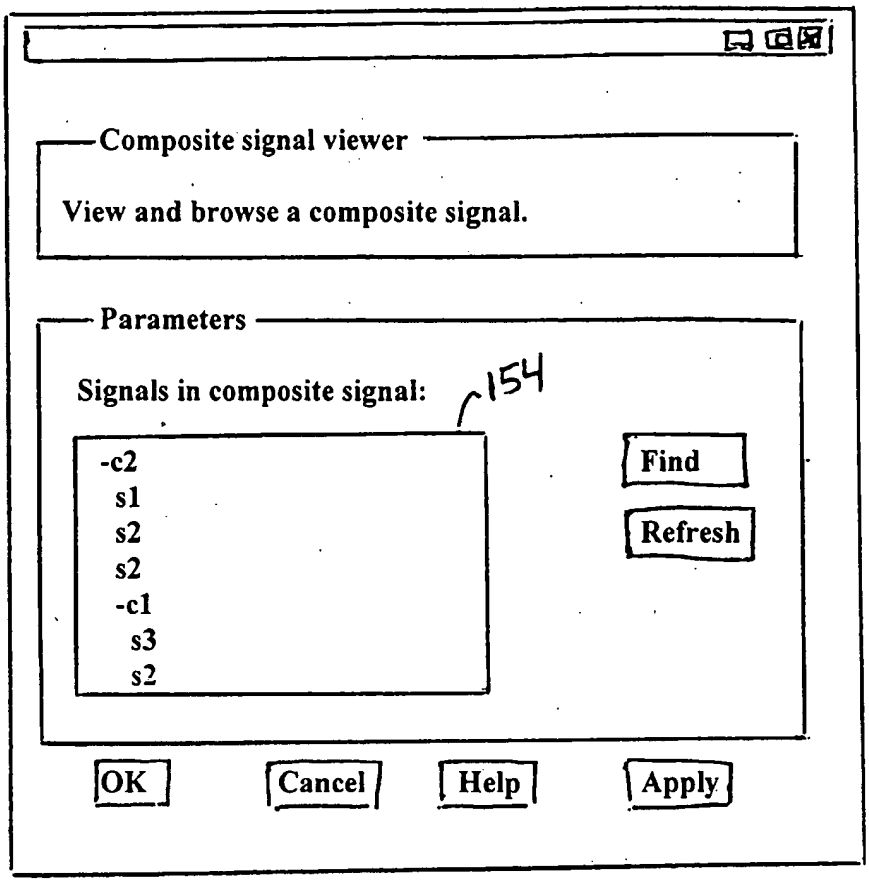


FIG. 9